Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently amended): A variable gain amplifier circuit comprising:

a plurality of common-emitter amplifier circuits which are different in voltage gain and employ bipolar transistors and

switch means for selecting the plurality of amplifier circuits, wherein:

the bases of the bipolar transistors are connected in common with each other; and the switch means are connected to the respective emitter sides of the bipolar transistors, and further wherein a collector current ratio between the plurality of amplifier circuits is inversely proportional to an emitter degeneration resistance ratio.

Claim 2 (Currently amended): A variable gain amplifier circuit comprising:

a plurality of amplifier circuits which are different in voltage gain and employ bipolar transistors and formed with a[[an]] common-emitter and common-base cascade connection and

switch means for selecting the plurality of amplifier circuits, wherein:

the bases of the common-emitter bipolar transistors are connected in common with each other; and the switch means are connected to the respective emitter sides of the bipolar transistors, and further wherein a collector current ratio between the plurality of amplifier circuits is inversely proportional to an emitter degeneration resistance ratio.

Claim 3 Canceled

Claim 4 (Currently amended): The variable gain amplifier circuit as ~~claimed~~ in claim 1 or ~~2~~3, wherein an emitter area ratio between common-emitter transistors in the plurality of amplifier circuits is inversely proportional to the emitter degeneration resistance ratio.

Claim 5 (Previously presented): The variable gain amplifier circuit as claimed in claim 4, wherein the emitter area ratio between the common-emitter transistors in the plurality of amplifier circuits is in powers of 2.

Claim 6 (Previously presented): The variable gain amplifier circuit as claimed in claim 4, wherein the emitter degeneration resistance ratio between the plurality of amplifier circuits is in powers of 2.

Claim 7 (Currently amended): A~~The~~ variable gain amplifier circuit comprising:

a plurality of common-source amplifier circuits which are different in voltage gain and employ field effect transistors and

switch means for selecting the plurality of amplifier circuits, wherein:

the gates of the field effect transistors are connected in common with each other; and

the switch means are connected to the respective source sides of the field effect transistors, and further wherein a drain current ratio between the plurality of amplifier circuits is inversely proportional to a source degeneration resistance ratio.

Claim 8 (Currently amended): A variable gain amplifier circuit comprising:

a plurality of amplifier circuits which are different in voltage gain and employ field effect transistors and formed with a common-source and common-gate cascade connection and

switch means for selecting the plurality of amplifier circuits, wherein:

the gates of the common-source field effect transistors are connected in common with each other; and the switch means are connected to the respective source sides of the field effect transistors, and further wherein a drain current ratio between the plurality of amplifier circuits is inversely proportional to a source degeneration resistance ratio.

Claim 9 Canceled

Claim 10 (Currently amended): A variable gain amplifier circuit comprising:

a plurality of common-source amplifier circuits which are different in voltage gain and employ field effect transistors and

switch means for selecting the plurality of amplifier circuits, wherein:

the gates of the field effect transistors are connected in common with each other;

the switch means are connected to the respective source sides of the field effect transistors; and~~The variable gain amplifier circuit as claimed in claim 7,wherein~~ a gate width ratio between common-source transistors in the plurality of amplifier circuits is inversely proportional to the source degeneration resistance ratio.

Claim 11 (Previously presented): The variable gain amplifier circuit as claimed in claim 10, wherein the gate width ratio between the common-source transistors in the plurality of amplifier circuits is in powers of 2.

Claim 12 (Previously presented): The variable gain amplifier circuit as claimed in claim 11, wherein the source degeneration resistance ratio between the plurality of amplifier circuits is in powers of 2.

Claim 13 (Previously presented): The variable gain amplifier circuit as claimed in claim 1, wherein the switch means is a current source.

Claim 14 (Previously presented): The variable gain amplifier circuit as claimed in claim 1, wherein the switch means is a transistor.

Claim 15 (Previously presented): The variable gain amplifier circuit as claimed in claim 1, wherein the switch means is an inverter.

Claim 16 (Previously presented): The variable gain amplifier circuit as claimed in claim 2, having bias circuits respectively corresponding to the plurality of amplifier circuits.

Claim 17 (Currently amended): A variable gain amplifier circuit comprising:

a plurality of amplifier circuits which are different in voltage gain and employ bipolar transistors and formed with a common-emitter and common-base cascade connection and

switch means for selecting the plurality of amplifier circuits, wherein:

the bases of the common-emitter bipolar transistors are connected in common with each other; and the switch means are connected to the respective emitter sides of the bipolar transistors, wherein the variable gain amplifier circuit further includes~~The variable gain amplifier~~

~~circuit as claimed in claim 2, having~~ a decoder as decoding means for receiving and decoding a digital signal and selecting any one of the plurality of amplifier circuits by its output corresponding to the digital signal received.

Claim 18 (Previously presented): The variable gain amplifier circuit as claimed in claim 17, having a decoder as decoding means for receiving and decoding a digital signal and selecting any combination of amplifier circuits by its output corresponding to the digital signal received.

Claim 19 (Previously presented): The variable gain amplifier circuit as claimed in claim 17, having decoding means for receiving and decoding a digital signal, including a first decoder for selecting one of the plurality of amplifier circuits by its output corresponding to the digital signal received and a second decoder for selecting any combination of amplifier circuits by its output corresponding to the digital signal received.

Claim 20 (Previously presented): A radio communication apparatus having the variable gain amplifier circuit as claimed in claim 1 as an amplifier circuit.